SOLID-STATE IMAGING DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-072820; filed March 31, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a solid-state imaging device.

BACKGROUND

A solid-state imaging device includes a semiconductor substrate, and the semiconductor substrate is divided into a pixel area and a circuit area. Pixels, each having a photoelectric conversion element and a plurality of transistors, are disposed in a matrix. A pixel drive unit, a signal processing unit, and the like are provided in the circuit area.

The pixel drive unit is configured with drivers or the like. The drivers are electrically coupled to transistors included in each pixel through drive signal lines. The drive signal lines are, for example, a select signal line, a reset signal line, and a transfer signal line.

The signal processing unit is configured by a column processing circuit and the like. The column processing circuit is coupled to a plurality of transistors included in pixels in each column by vertical signal lines.

Drive signals which are output from the driver are supplied to the transistors through the drive signal lines. Accordingly, the transistors operate, and reading of a pixel signal or the like is performed. As the pixel signal which is output from an amplification transistor is supplied to the column processing circuit through the vertical signal line, the reading of the pixel signal is performed.

Since this type of a solid-state imaging device receives lots of light, the pixel area increases. According to this, an amount of pixel signals which are processed in the pixel area and the circuit area increases, and thus the circuit area tends to increase, but, on the other hand, a small-sized device is required. For this reason, there is a limit to a structure in which a pixel area and a circuit area are provided on the same semiconductor substrate. Thus, it is known a structure of a solid-state imaging device in which a pixel area and a circuit area are separately provided on a semiconductor substrate and are disposed in an overlapping manner.

In a structure in which semiconductor substrates are disposed in an overlapping manner, a coupling portion which electrically couples electrodes provided on each semiconductor substrate is configured, and thereby a pixel area is electrically coupled to a circuit area. Through the coupling portion, a drive signal which is output from the driver can be supplied to a transistor included in a pixel. In addition, a pixel signal which is output from the transistor can be supplied to a signal processing unit. In this way, coupling portions corresponding to the number of transistors which receives and outputs a signal are required.

An example of related art includes JP-A-2012-54876.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic exploded perspective view illustrating a configuration of a solid-state imaging device according to a first embodiment.

FIG. 2 is a schematic top diagram illustrating a part of a configuration of the solid-state imaging device according to the first embodiment.

FIG. 3 is a schematic sectional diagram illustrating a structure of the solid-state imaging device according to the first embodiment.

FIG. 4 is an equivalent circuit illustrating a part of a configuration of the solid-state imaging device according to the first embodiment.

FIGS. 5A and 5B are other equivalent circuits illustrating a part of a configuration of the solid-state imaging device according to the first embodiment.

FIG. 6 is a timing chart illustrating an operation of the solid-state imaging device according to the first embodiment.

FIG. 7 is a schematic top diagram illustrating a part of a configuration of a solid-state imaging device according to a second embodiment.

FIG. 8 is a timing chart illustrating an operation of the solid-state imaging device according to the second embodiment.

FIG. 9 is a schematic top diagram illustrating a part of a configuration of a solid-state imaging device according to a third embodiment.

FIG. 10 is a schematic top diagram illustrating a part of a configuration of a solid-state imaging device according to a fourth embodiment.

DETAILED DESCRIPTION

[0009]Exemplary embodiments provide a solid-state imaging device which can reduce the number of coupling portions of a stacked structure.

[0010]According to one embodiment, a solid-state imaging device includes a first pixel group which is provided on a first semiconductor substrate and has pixels including photoelectric conversion elements; a second pixel group which has pixels including photoelectric conversion elements; a first electrode; a first switching element which is coupled to the first electrode; a first latch circuit which is coupled to the first switching element and the first pixel group; a second switching element which is coupled to the first electrode; a second latch circuit which is coupled to the second switching element and the second pixel group; a second electrode that is provided on a second semiconductor substrate on which the first semiconductor substrate is stacked, and is coupled to the first electrode; a driver which is coupled to the second electrode; and a control unit which operates the first switching element, the second switching element, the first latch circuit, and the second latch circuit.

[0012]A first embodiment will be hereinafter described with reference to the accompanying drawings. In each drawing, the same symbols or reference numerals will be attached to the same configuration elements, and detailed description thereof will be appropriately omitted.

First Embodiment

[0013]A solid-state imaging device according to a first embodiment will be described with reference to FIG. 1 to FIG. 6. FIG. 1 is a schematic exploded perspective view illustrating a configuration of a solid-state imaging device according to a first embodiment. FIG. 2 is a schematic top diagram illustrating a part of a configuration of the solid-state imaging device according to the first embodiment. FIG. 3 is a schematic sectional diagram illustrating a structure of the solid-state imaging device according to the first embodiment. FIG. 4 is an equivalent circuit illustrating a part of a configuration of the solid-state imaging device according to the first embodiment. FIGS. 5A and 5B are other equivalent circuits illustrating a part of a configuration of the solid-state imaging device according to the first embodiment. FIG. 6 is a timing chart illustrating an operation of the solid-state imaging device according to the first embodiment.

[0014]The solid-state imaging device according to the first embodiment is configured by a first semiconductor substrate 1 and a second semiconductor substrate 10 which are disposed in an overlapping manner, as illustrated in FIG. 1. The first semiconductor substrate 1 and the second semiconductor substrate 10 are semiconductor substrates which are separated from each other.

[0015]The solid-state imaging device according to the first embodiment is divided into a first semiconductor substrate 1 and a second semiconductor substrate 10, and the structures thereof will be respectively described.

[0016]As illustrated in FIG. 1, the first semiconductor substrate 1 includes a pixel area 2, a switching element 3, and a latch circuit 4. The second semiconductor substrate 10 includes a control unit 12, a pixel drive unit 14, and a signal processing unit 15. Meanwhile, in the first embodiment, an example in which the control unit 12 is provided on the second semiconductor substrate 10 is described, but the control unit 12 may be provided on the first semiconductor substrate 1. In the first semiconductor substrate 1 and the second semiconductor substrate 10, a coupling portion 25 is configured by electrically coupling a first electrode 25a provided on the first semiconductor substrate to a second electrode 25b provided on the second semiconductor substrate. Pixels 6 provided on the first semiconductor substrate 1 are electrically coupled to the pixel drive unit 14 and the signal processing unit 15 which are provided on the second semiconductor substrate 10 by the coupling portion 25. Here, providing the electrode on the first semiconductor substrate 1 means not only that the electrode is directly provided on the first semiconductor substrate 1, but also that the electrode is upwardly provided on the first semiconductor substrate 1 without coming into direct contact with the first semiconductor substrate 1. That is, providing the electrode on the first semiconductor substrate 1 also means that, for example, a multilayer wiring layer, an interlayer insulating film, or the like which will be described later is interposed between the first semiconductor substrate 1 and the electrode. In addition, this case is not limited to the electrode, and may also be applied to the switching element 3, the latch circuit 4, or the like.

[0017]The first semiconductor substrate 1 and the second semiconductor substrate 10 will be described with reference to FIG. 2.

[0018]The first semiconductor substrate 1 includes the pixel area 2, the switching element 3, the latch circuit 4, and the first electrode 25a.

[0019]The pixel area 2 is configured by a plurality of pixels 6 which are disposed in a matrix.

[0020]In the first embodiment, a collection of the pixels 6 which are disposed in a first row of the pixel area 2 is referred to as a first pixel group 6a. A collection of the pixels 6 which are disposed in a second row of the pixel area 2 is referred to as a second pixel group 6b. The second pixel group 6b is disposed in parallel with the first pixel group 6a. In the first embodiment, for the sake of clear description, only the first pixel group 6a and the second pixel group 6b are described, but, in the same manner, a collection of the pixels 6 which are disposed in an nth row is referred to as an nth pixel group.

[0021]The pixel 6 is configured with a photo diode 7 serving as a photoelectric conversion element which generates and accumulates signal charges corresponding to an amount of received light, and a plurality of transistors 8 which reads the signal charges generated by the photo diode 7 and outputs the read signal charges as a pixel signal. The transistors 8 include a select transistor 8a, a reset transistor 8b, a transfer transistor 8c, and an amplification transistor 8d. Meanwhile, the select transistor 8a may be removed from a configuration of the transistors 8. In the present embodiment, an example in which the transistors 8 included in the pixel 6 are configured by the select transistor 8a, the reset transistor 8b, the transfer transistor 8c, and the amplification transistor 8d is described. Meanwhile, a circuit configuration of the pixel 6 will be described later.

[0022]The switching element 3 is configured by a first switching element 3a and a second switching element 3b. The first switching element 3a couples the first pixel group 6a to the pixel drive unit 14 which will be described later, or decouples the first pixel group 6a from the pixel drive unit 14. One terminal of the first switching element 3a is coupled to the first electrode 25a, and the other terminal of the first switching element 3a is coupled to a first latch circuit 4a which will be described later. The second switching element 3b couples the second pixel group 6b to the pixel drive unit 14 which will be described later, or decouples the second pixel group 6b from the pixel drive unit 14. One terminal of the second switching element 3b is coupled to the first electrode 25a, and the other terminal of the second switching element 3b is coupled to a second latch circuit 4b which will be described later. The switching element 3 is, for example, one of an NMOS transistor and a PMOS transistor, or a transmission gate in which an NMOS transistor and a PMOS transistor are coupled in parallel. In the first embodiment, an example in which a transmission gate that operates at a high speed is used as the switching element 3 will be described. Meanwhile, detailed description of the switching element 3 will be made later.

[0023]The latch circuit 4 is configured with the first latch circuit 4a corresponding to the first switching element 3a and the second latch circuit 4b corresponding to the second switching element 3b. After the first switching element 3a is turned off and the first pixel group 6a is decoupled from the pixel drive unit 14, the first latch circuit 4a retains a drive signal before the first switching element 3a is turned off. One terminal of the first latch circuit 4a is coupled to the first switching element 3a, and the other terminal of the first latch circuit 4a is coupled to the first pixel group 6a. After the second switching element 3b is turned off and the second pixel group 6b is decoupled from the pixel drive unit 14, the second latch circuit 4b retains a drive signal before the second switching element 3b is turned off. One terminal of the second latch circuit 4b is coupled to the second switching element 3b, and the other terminal of the second latch circuit 4b is coupled to the second pixel group 6b. The latch circuit 4 is a circuit in which a CMOS inverter 5a and a clocked inverter 5b are coupled in parallel. In the first embodiment, an example in which a circuit that is configured by coupling the CMOS inverter 5a and the clocked inverter 5b in parallel is used as the latch circuit 4 is described. Meanwhile, detailed description of the latch circuit 4 will be made later.

[0024]The second semiconductor substrate 10 includes the control unit 12, the pixel drive unit 14, the signal processing unit 15, and the second electrode 25b.

[0025]The control unit 12 is configured with a first control driver 12a which operates the first switching element 3a and the first latch circuit 4a, and a second control driver 12b which operates the second switching element 3b and the second latch circuit 4b.

[0026]The first control driver 12a is electrically coupled to the first switching element 3a and the first latch circuit 4a through a control signal line 26. The control signal line 26 is divided into a first control signal line 26a and a second control signal line 26b on the first semiconductor substrate 1 through the first electrode 25a and the second electrode 25b. The first control signal line 26a is electrically coupled to a gate of a PMOS transistor configuring the first switching element 3a, and the first latch circuit 4a. The second control signal line 26b is electrically coupled to a gate of an NMOS transistor configuring the first switching element 3a, and the first latch circuit 4a through an inverter 18.

[0027]The second control driver 12b is electrically coupled to the second switching element 3b and the second latch circuit 4b through the control signal line 26. The control signal line 26 is divided into the first control signal line 26a and the second control signal line 26b on the first semiconductor substrate 1 through the first electrode 25a and the second electrode 25b. The first control signal line 26a is electrically coupled to a gate of a PMOS transistor configuring the second switching element 3b, and the second latch circuit 4b. The second control signal line 26b is electrically coupled to a gate of an NMOS transistor configuring the second switching element 3b, and the second latch circuit 4b through the inverter 18.

[0028]Meanwhile, in the first embodiment, an example in which the control unit 12 is provided on the second semiconductor substrate 10 is described, but the control unit 12 may be provided on the first semiconductor substrate 1. In addition, the control unit 12 has a function of respectively outputting timing signals to the pixel drive unit 14 and the signal processing unit 15 which will be described later.

[0029]The pixel drive unit 14 is configured by a decoder (not illustrated), a plurality of drivers 13, or the like. The drivers 13 are disposed such that one driver 13 corresponds to pixel groups in two rows. In the first embodiment, an example in which one driver 13 that operates the first pixel group 6a and the second pixel group 6b is referred to as a first driver 13a is described. The first driver 13a is coupled to a drive signal line which will be described later.

[0030]The first driver 13a includes a select signal driver sel13a which operates the select transistor 8a included in the pixel 6, a reset signal driver res13a which operates the reset transistor 8b included in the pixel 6, and a transfer signal driver tx13a which operates the transfer transistor 8c included in the pixel 6. The select signal driver sel13a outputs a select signal to the select transistor 8a through a select signal line 21. The reset signal driver res13a outputs a reset signal to the reset transistor 8b through a reset signal line 22. The transfer signal driver tx13a outputs a transfer signal to the transfer transistor 8c through a transfer signal line 23. In the first embodiment, in order to avoid complication of the drawings, the select signal driver sel13a, the reset signal driver res13a, and the transfer signal driver tx13a are collectively referred to as the first driver 13a. When the signals are described without distinguishing, a select signal sel, a reset signal res, and a transfer signal tx are collectively referred to as drive signals. In addition, the signal lines of the select signal line 21, the reset signal line 22, and the transfer signal line 23 are collectively referred to as drive signal lines.

[0031]The drive signal lines are coupled to the second electrode 25b. The drive signal lines are divided on the first semiconductor substrate 1 through the first electrode 25a and the second electrode 25b, and are respectively coupled to the first pixel group 6a and the second pixel group 6b. By doing so, in the solid-state imaging device having a stacked structure, the first driver 13a coupled to the drive signal line is electrically coupled to the first pixel group 6a and the second pixel group 6b through the first electrode 25a and the second electrode 25b. Hereinafter, the description will be omitted, but the driver 13 which operates a third pixel group 6c and a fourth pixel group 6d is a second driver 13b, and the driver 13 which operates a fifth pixel group 6e and a sixth pixel group 6f is a third driver 13c. In addition, each drive signal line is also divided on the first semiconductor substrate 1 through the first electrode 25a and the second electrode 25b, and electrically couples a corresponding pixel group to the driver 13.

[0032]The signal processing unit 15 includes correlated double sampling (CDS) circuits 16 or AD conversion circuits (not illustrated).

[0033]The CDS circuits 16 are provided for each column of the pixels 6. The CDS circuits 16 are electrically coupled to the pixels through vertical signal lines 24.

[0034]The CDS circuits 16 takes a difference between a reset voltage and a pixel voltage which are output from the amplification transistor 8d, and removes noise included in the pixel signal. Thereafter, a scan circuit which is not illustrated outputs a signal, and thereby a pixel signal from an AD conversion circuit is output to a horizontal signal line.

[0035]In the first semiconductor substrate 1 and the second semiconductor substrate 10 which have the aforementioned configurations, the pixel area 2, the pixel drive unit 14, and the signal processing unit 15 are coupled to each other through the first electrode 25a and the second electrode 25b.

[0036]Subsequently, a configuration of the coupling portion 25 which couples the pixel area 2, the pixel drive unit 14, and the signal processing unit 15 to each other will be described as follows.

[0037]A surface of the first semiconductor substrate 1 on which a photoelectric conversion element provided on the first semiconductor substrate 1 receives light is referred to as a lower surface, and a surface opposite to the lower surface is referred to as an upper surface. In addition, a surface of the second semiconductor substrate 10 which overlap the first semiconductor substrate 1 is referred to as an upper surface, and a surface opposite to the upper surface is referred to as a lower surface.

[0038]A multilayer wiring layer is provided on the first semiconductor substrate 1 (not illustrated). In the multilayer wiring layer, transistors or a plurality of wires are covered with an insulating film or the like (not illustrated). Furthermore, in the multilayer wiring layer, contacts which couple wires adjacent to each other are provided in a direction from the lower surface toward the upper surface (not illustrated). A wire which is exposed from a top surface of the multilayer wiring layer is referred to as the first electrode 25a.

[0039]A multilayer wiring layer is provided on the second semiconductor substrate 10 (not illustrated). In the multilayer wiring layer, transistors configuring the pixel drive unit 14 and the signal processing unit 15, or a plurality of wires are covered with an insulating film (not illustrated). A wire which is exposed from a top surface of the multilayer wiring layer is referred to as the second electrode 25b. Furthermore, in the multilayer wiring layer, contacts which couple wires adjacent to each other are provided in a direction from the lower surface toward the upper surface (not illustrated). The wire which is exposed from the top surface of the multilayer wiring layer is referred to as the second electrode 25b.

[0040]As the first semiconductor substrate 1 overlap the second semiconductor substrate 10, the first electrode 25a is electrically coupled to the second electrode 25b, and thereby the coupling portion 25 is configured. By doing so, the pixels 6 provided on the first semiconductor substrate 1 are electrically coupled to the pixel drive unit 14 and the signal processing unit 15 which are provided on the second semiconductor substrate 10. Thus, drive signals which are output by the pixel drive unit 14 are respectively supplied to the transistors 8. In addition, the pixel signal which is output from the pixel 6 is supplied to the signal processing unit 15 through the coupling portion 25.

[0041]Subsequently, a circuit configuration of the pixel 6 will be described with reference to FIG. 4.

[0042]As described in FIG. 4, the pixel 6 includes the photo diode 7 serving as a photoelectric conversion element, and the plurality of transistors 8. In the first embodiment, an example in which the plurality of transistors 8 are configured by the select transistor 8a, the reset transistor 8b, the transfer transistor 8c, and the amplification transistor 8d is described, but the select transistor 8a may be removed from the plurality of transistors 8. In the first embodiment, an example in which the transistors 8 are configured by NMOS transistors is described.

[0043]A drain of the select transistor 8a is coupled to a source of the amplification transistor 8d, and a source of the select transistor 8a is electrically coupled to the signal processing unit 15 through the vertical signal line 24. A gate of the select transistor 8a is electrically coupled to the driver 13 included in the pixel drive unit 14 through the select signal line 21. The select transistor 8a selects the pixel 6 which performs reading in response to the select signal driver sel13a which is output from the driver 13.

[0044]A drain of the reset transistor 8b is coupled to a power supply terminal 17, and a source of the reset transistor 8b is coupled to a gate of the amplification transistor 8d through a floating diffusion node (hereinafter, referred to as FD) 9. The gate of the reset transistor 8b is electrically coupled to the driver 13 included in the pixel drive unit 14 through the reset signal line 22. The reset transistor 8b increases a potential of the FD 9 to a voltage VDD of the power supply terminal 17 in response to a reset signal res13b which is output from the driver 13. This potential becomes a reset potential.

[0045]A drain of the transfer transistor 8c is coupled to a gate of the amplification transistor 8d through the FD 9. A source of the transfer transistor 8c is coupled to the photo diode 7. A gate of the transfer transistor 8c is electrically coupled to the driver 13 included in the pixel drive unit 14 through the transfer signal line 23. The transfer transistor 8c transfers electric charges accumulated in the photo diode 7 to the FD 9 in response to a transfer signal tx13c which is output from the driver 13. By doing so, the potential of the FD 9 decreases by a potential corresponding to the electric charges accumulated in the photo diode 7 from the reset potential. This potential becomes a pixel potential.

[0046]A drain of the amplification transistor 8d is coupled to the power supply terminal 17, and a source of the amplification transistor 8d is coupled to a drain of the select transistor 8a. A gate of the amplification transistor 8d is coupled to the FD 9. The amplification transistor 8d amplifies the potential of the FD 9, and outputs a voltage corresponding to the potential to the vertical signal lines 24.

[0047]Hereinafter, the select signal line 21, the reset signal line 22, and the transfer signal line 23 are collectively referred to as drive signal lines.

[0048]Subsequently, circuit configurations of the switching element 3 and the latch circuit 4 will be described with reference to FIG. 5A.

[0049]An example of the switching element 3 will be described by using the first switching element 3a. In addition, in the same manner, an example of the latch circuit 4 will also be described by using the first latch circuit 4a. The second switching element 3b and the second latch circuit 4b also have the same structures.

[0050]In the first embodiment, the first switching element 3a will be described by using a transmission gate.

[0051]The transmission gate is a circuit in which a drain of a PMOS transistor and a drain of an NMOS transistor are shared and a source of the PMOS transistor and a source of the NMOS transistor are shared.

[0052]A gate of a PMOS transistor of the first switching element 3a is electrically coupled to the first control signal line 26a, and a gate of an NMOS transistor of the first switching element 3a is electrically coupled to the control unit 12 through the second control signal line 26b.

[0053]If a control signal “0” having a low level is input to a gate of the PMOS transistor and a control signal “1” having a high level is input to a gate of the NMOS transistor, the first switching element 3a couples a pixel group to the pixel drive unit 14.

[0054]Meanwhile, if a control signal “1” having a high level is input to the gate of the PMOS transistor and a control signal “0” having a low level is input to the gate of the NMOS transistor, the first switching element 3a decouples a pixel group from the pixel drive unit 14.

[0055]Subsequently, the first latch circuit 4a will be described.

[0056]The first latch circuit 4a is a circuit in which, for example, a CMOS inverter 5a and a clocked inverter 5b are coupled in parallel.

[0057]In the first embodiment, a circuit in which the CMOS inverter 5a and the clocked inverter 5b are coupled in parallel will be described as an example of the first latch circuit 4a.

[0058]The CMOS inverter 5a is a circuit in which a gate of a PMOS transistor p1 and a gate of an NMOS transistor n1 are shared and a source of the PMOS transistor p1 and a drain of the NMOS transistor n1 are shared.

[0059]A gate side of the CMOS inverter 5a is set as an input point A, and a point in which the soured of the PMOS transistor p1 and the drain of the NMOS transistor n1 are shared is set as an output point B.

[0060]The input point A of the CMOS inverter 5a is electrically coupled to the driver 13 through the drive signal line.

[0061]When the switching element 3 is turned on, the drive signal from the driver 13 is input to the input point A of the CMOS inverter 5a.

[0062]The output point B of the CMOS inverter 5a is electrically coupled to the transistors 8 included in the pixel 6 and the clocked inverter 5b through the drive signal line.

[0063]The output point B of the CMOS inverter 5a outputs a drive signal which is obtained by inverting the drive signal that is input to the CMOS inverter 5a.

[0064]The clocked inverter 5b is configured with two PMOS transistors p2 and p3, and two NMOS transistors n2 and n3.

[0065]The clocked inverter 5b is a circuit in which a gate of the PMOS transistor p2 and a gate of the NMOS transistor n3 are set as an input point X in a shared manner and a source of the PMOS transistor p3 and a drain of the NMOS transistor n2 are set as an output point Y in a shared manner.

[0066]A drain of the PMOS transistor p2 is coupled to the power supply terminal 17, and a source of the PMOS transistor p2 is coupled to a drain of the PMOS transistor p3. A gate of the PMOS transistor p2 is coupled to the drive signal line.

[0067]The drain of the PMOS transistor p3 is coupled to the source of the PMOS transistor p2, and the source of the PMOS transistor p3 is coupled to the drain of the NMOS transistor n2. A gate of the PMOS transistor p3 is electrically coupled to the control unit 12 through the second control signal line 26b.

[0068]The drain of the NMOS transistor n2 is coupled to the source of the PMOS transistor p3, and a source of the NMOS transistor n2 is coupled to a drain of the NMOS transistor n3. The gate of the NMOS transistor n2 is electrically coupled to the control unit 12 through the first control signal line 26a.

[0069]A drain of the NMOS transistor n3 is coupled to the source of the NMOS transistor n2, and a source of the NMOS transistor n3 is grounded. The gate of the NMOS transistor n3 is coupled to the drive signal line.

[0070]A control signal is input to one of the gate of the PMOS transistor p3 and the gate of the NMOS transistor n2, and a signal which is symmetric with respect to the control signal is input to the other of the gate of the PMOS transistor p3 and the gate of the NMOS transistor n2. Thus, if the control signal “0” having a low level is input to the gate of the PMOS transistor p3 and the control signal “1” having a high level is input to the gate of the NMOS transistor n2, the PMOS transistor p3 and the NMOS transistor n2 are turned on. Accordingly, the clocked inverter 5b is turned on.

[0071]In this state, the drive signal “0” having a low level which is output from the CMOS inverter 5a is input to the gate of the PMOS transistor p2 and the gate of the NMOS transistor n3. Accordingly, the PMOS transistor p2 is turned on, and the NMOS transistor n3 is turned off. At this time, the drive signal “1” having a high level is output from the output point Y. Furthermore, the drive signal “1” having a high level is input to the CMOS inverter 5a, and the drive signal “0” having a low level is output from the CMOS inverter 5a. By repeating the stat, a signal is retained by the latch circuit 4.

[0072]Meanwhile, if the control signal “1” having a high level is input to the gate of the PMOS transistor p3 and the control signal “0” having a low level is input to the gate of the NMOS transistor n2, the PMOS transistor p2 and the NMOS transistor n3 are turned off. Accordingly, the clocked inverter 5b is turned off. The first switching element 3a and the first latch circuit 4a are illustrated in FIG. 5B.

[0073]Subsequently, the first control driver 12a and the second control driver 12b which are included in the control unit 12 will be described with reference to FIG. 2. The first control driver 12a is electrically coupled to the first switching element 3a and the first latch circuit 4a through the control signal line 26.

[0074]In the first embodiment, the control signal line 26 is divided into the first control signal line 26a and the second control signal line 26b on the first semiconductor substrate 1.

[0075]The first control signal line 26a is electrically coupled to a gate of a PMOS transistor of the first switching element 3a, and the first latch circuit 4a.

[0076]The second control signal line 26b is electrically coupled to a gate of an NMOS transistor of the first switching element 3a, and the second latch circuit 4b through an inverter 18.

[0077]As described above, when the first switching element 3a is turned on, the first latch circuit 4a is turned off, and when the first switching element 3a is turned off, the first latch circuit 4a is turned on.

[0078]Subsequently, an operation of the solid-state imaging device according to the first embodiment will be described.

[0079]In the solid-state imaging device according to the first embodiment, one or both of the first switching element 3a and the second switching element 3b which are designated by the control unit 12 are turned on or off. When the first switching element 3a is turned on and the second switching element 3b is turned off, the first pixel group 6a and the first driver 13a are coupled to each other. When the first switching element 3a is turned off and the second switching element 3b is turned on, the second pixel group 6b and the first driver 13a are coupled to each other. In addition, when the first switching element 3a and the second switching element 3b are turned on, both the first pixel group 6a and the second pixel group 6b are coupled to the first driver 13a. If one or both of the first pixel group 6a and the second pixel group 6b is coupled to the first driver 13a, the first driver 13a outputs a drive signal to the select transistor 8a, the reset transistor 8b, and the transfer transistor 8c which are included in each pixel 6. The latch circuit 4 retains a drive signal before the switching element 3 is turned off.

[0080]The pixel group which is coupled to the first driver 13a outputs a pixel signal to the vertical signal lines 24. The vertical signal lines 24 supplies the pixel signal to the signal processing unit 15 through the coupling portion 25. The signal processing unit 15 performs a digital conversion or the like of the received pixel signal, and outputs the converted signal to an external device.

[0081]A specific operation of the solid-state imaging device according to the first embodiment will be described with reference to FIG. 2, FIG. 4, FIGS. 5A and 5B, and FIG. 6.

[0082]Here, a case in which one of the first pixel group 6a and the second pixel group 6b is coupled to the first driver 13a will be described.

[0083]At time T1 illustrated in FIG. 6, the control signal of the first control driver 12a is set to a voltage “0” having a low level. By doing so, the first switching element 3a is turned on, and the first driver 13a is coupled to the first pixel group 6a.

[0084]When the first control driver 12a outputs the control signal “0” having a low level, the first latch circuit 4a is turned on.

[0085]In addition, at time T1, the second control driver 12b sets the control signal to a voltage “1” having a high level. By doing so, the second switching element 3b is turned off, and the first driver 13a is decoupled from the transistor 8 included in the second pixel group 6b.

[0086]At time T2, in a state in which the first switching element 3a is turned on, the select signal sel13a “0” which is an inverted signal of the select signal sel13a “1” that operates the select transistor 8a is output from the first driver 13a. The select signal sel13a “0” is inverted to the select signal sel13a “1” by the CMOS inverter 5a included in the first latch circuit 4a, and is input to the select transistor 8a included in the first pixel group 6a. By doing so, the select transistor 8a to which the select signal sel13a “1” is input operates.

[0087]At time T3, in a state in which the first switching element 3a is turned on, the reset signal res13a “0” which is an inverted signal of the reset signal res13a “1” that operates the reset transistor 8b is output from the first driver 13a. The reset signal res13a “0” is inverted to the reset signal res13a “1” by the CMOS inverter 5a included in the first latch circuit 4a, and is input to the reset transistor 8b included in the first pixel group 6a. By doing so, the reset transistor 8b to which the reset signal res13a “1” is input operates, and the potential of the FD 9 becomes a potential VDD of the power supply terminal 17. A voltage of the FD 9 corresponding to the power supply terminal 17 becomes a reset potential. The reset voltage is applied to a gate of the amplification transistor 8d, and is output to the vertical signal lines 24 through the select transistor 8a. The reset voltage is input to the signal processing unit 15 through the vertical signal lines 24.

[0088]At time T4, the reset signal res13a is set to a voltage “0” having a low level, and an inverted reset signal res13a “1” is output. The reset signal res13a “0” which is inverted by the CMOS inverter 5a included in the first latch circuit 4a is input to the reset transistor 8b. By doing so, the reset transistor 8b stops.

[0089]Subsequently, at time T5, in a state in which the first switching element 3a is turned on, the transfer signal tx13a “0” which is an inverted signal of the transfer signal tx13a “1” that operates the transfer transistor 8c is output from the first driver 13a. The transfer signal tx13a “0” is inverted to the transfer signal tx13a “1” by the CMOS inverter 5a included in the first latch circuit 4a, and is input to the transfer transistor 8c included in the first pixel group 6a. By doing so, the transfer transistor 8c to which the transfer signal tx13a “1” is input operates.

[0090]As the transfer transistor 8c operates, the electric charges accumulated in the photo diode 7 are transferred to the FD 9. The electric charges are applied to a gate of the amplification transistor 8d as a pixel voltage. The pixel voltage is output to the vertical signal lines 24 through the select transistor 8a, and thereafter, the pixel voltage is input to the signal processing unit 15.

[0091]The signal processing unit 15 takes a difference between the reset voltage and the pixel voltage thereby removing noise. After that, digital conversion of the signal is performed by a circuit (not illustrated) having an AD conversion function.

[0092]At time T6 when reading of the electric charges of the photo diode 7 is completed, the transfer signal tx13a is set to a voltage “0” having a low level, and the inverted transfer signal tx13a “1” is output. In the same manner as the reset signal res13a, the transfer signal tx13a is input to the transfer transistor 8c included in the first pixel group 6a. By doing so, the transfer transistor 8c stops. Accordingly, the reset state is maintained.

[0093]Subsequently, at time T7, if the control signal of the first control driver 12a is set to a voltage “1” having a high level, the first switching element 3a is turned off. By doing so, the first driver 13a is decoupled from the first pixel group 6a.

[0094]In addition, the first latch circuit 4a is turned off in accordance with the control signal which is output from the first control driver 12a. Here, an operation of the first latch circuit 4a will be described with reference to FIG. 5A. When the first latch circuit 4a is in an ON state, the transfer signal tx13a “0” is input from the input point X of the clocked inverter 5b before the first switching element 3a is turned off. The transfer signal “0” which is input to the clocked inverter 5b is inverted, and the transfer signal “1” is output from the output point Y. Furthermore, the transfer signal tx13a “1” is input to the CMOS inverter, and an inverted transfer signal tx13a “0” is output. By repeating the above operations, the first latch circuit 4a retains the transfer signal tx13a. Accordingly, the transfer transistor 8c stops, and maintains a reset state.

[0095]At time T7, the second control driver 12b sets the control signal to a voltage “0” having a low level. By doing so, the second switching element 3b is turned on, and the first driver 13a is coupled to the transistors 8 included in the second pixel group 6b.

[0096]The second pixel group 6b also performs the same operation as the first pixel group 6a.

[0097]The solid-state imaging device according to the first embodiment includes the switching element 3 and the latch circuit 4 which are provided on the first semiconductor substrate 1. By doing so, one or both of the first switching element 3a and the second switching element 3b which are included in the switching element 3 are turned on, and thereby one or both of the first pixel group 6a and the second pixel group 6b which correspond to those are coupled to the first driver 13a. Accordingly, it is possible for the first driver 13a to operate each pixel group. That is, one driver can operate two pixel groups, and thus it is possible to reduce the number of drive signal lines which couple the drivers 13 to the pixel groups. For this reason, it is possible to reduce the number of the coupling portions 25 which are configured by overlapping the first semiconductor substrate 1 with the second semiconductor substrate 10.

[0098]In the solid-state imaging device according to the first embodiment, for example, the number of the coupling portions 25 required to couple the driver 13 and the control unit 12 which are provided on the second semiconductor substrate 10 to the elements which are provided on the first semiconductor substrate 1 can be represented by Expression 1.

[0099]When the number of pixel groups is n, the number T of the coupling portions is represented by Expression 1.

(Expression 1) T=n/(2+2)

[0100]For example, as described in the example of the first embodiment, in a case of two pixel groups, the number of the coupling portions 25 at the time when the driver 13 and the control unit 12 are coupled to the elements provided on the first semiconductor substrate 1 is three pieces.

[0101]In the first embodiment, only the first driver 13a, the first pixel group 6a, and the second pixel group 6b are described, but one driver 13 can operate two pixel groups, also in the second driver 13b and the third driver 13c as well as the first driver 13a, and thus it is possible to reduce the number of the coupling portions 25.

Second Embodiment

[0102]A solid-state imaging device according to a second embodiment will be described with reference to FIG. 7 and FIG. 8. FIG. 7 is an equivalent circuit diagram illustrating a pixel area and a circuit area of the solid-state imaging device according to the second embodiment. FIG. 8 is a timing chart illustrating an operation of the solid-state imaging device according to the second embodiment.

[0103]The solid-state imaging device according to the second embodiment is different from the solid-state imaging device according to the first embodiment in that one driver 13 can operate the first pixel group 6a, the second pixel group 6b, and the third pixel group 6c. That is, it is possible to further reduce the number of the coupling portions 25 which electrically couple the first semiconductor substrate 1 to the second semiconductor substrate 10. Since the solid-state imaging device according to the second embodiment is the same as that according to the first embodiment except for the above-described point, the same symbols or reference numerals will be attached to the same portions, and detailed description thereof will be omitted.

[0104]A structure of the solid-state imaging device according to the second embodiment will be described.

[0105]Drivers which outputs drive signals corresponding to each transistor to the select transistor 8a, the reset transistor 8b, and the transfer transistor 8c which are included in each pixel group is referred as a first driver 13a. The first driver 13a is coupled to the first pixel group 6a, the second pixel group 6b, and the third pixel group 6c through a drive signal line. The drive signal line is divided into three drive signal lines on the first semiconductor substrate 1 through the coupling portion 25, and the three drive signal lines are coupled to each pixel group.

[0106]The switching element 3 is configured with a first switching element 3a which is coupled to the first pixel group 6a, a second switching element 3b which is coupled to the second pixel group 6b, and a third switching element 3c which is coupled to the third pixel group 6c. In the second embodiment, the switching element 3 is, for example, one of an NMOS transistor and a PMOS transistor, or a transmission gate in which an NMOS transistor and a PMOS transistor are coupled in parallel. In the second embodiment, the transmission gate will be described as an example of the switching element 3 in the same manner as in the first embodiment.

[0107]The latch circuit 4 is configured with a first latch circuit 4a corresponding to the first switching element 3a, a second latch circuit 4b corresponding to the second switching element 3b, and a third latch circuit 4c corresponding to a third switching element 3c. In the second embodiment, a circuit in which the CMOS inverter 5a and the clocked inverter 5b are coupled in parallel will be described as an example of the latch circuit 4.

[0108]Description of the structures of the switching element 3 and the latch circuit 4 will be omitted.

[0109]The switching element 3 and the latch circuit 4 are provided on the first semiconductor substrate 1 in the same manner as in the solid-state imaging device according to the first embodiment.

[0110]A control unit 12 is configured with the first control driver 12a which operates the first switching element 3a and the first latch circuit 4a, the second control driver 12b which operates the second switching element 3b and the second latch circuit 4b, and a third control driver 12c which operates a third switching element 3c and a third latch circuit 4c. In addition, the control unit 12 respectively outputs timing signals to the pixel drive unit 14 and the signal processing unit 15.

[0111]The control signal line 26 through which a control signal that is output from the control unit 12 is transferred is divided into the first control signal line 26a and the second control signal line 26b on the first semiconductor substrate 1 through the coupling portion 25.

[0112]Subsequently, an operation of the solid-state imaging device according to the second embodiment will be described with reference to FIG. 7 and FIG. 8.

[0113]Meanwhile, an operation of the transistors 8 included in each pixel 6 is the same as that of the first embodiment, and thus detailed description thereof will be omitted. In addition, here, only a case in which one of the first pixel group 6a, the second pixel group 6b, and the third pixel group 6c is coupled to the first driver 13a will be described, but a case in which two of the pixel groups is coupled to the first driver 13a, or a case in which the entire pixel groups are coupled to the first driver 13a may also be realized.

[0114]At time T1 illustrated in FIG. 8, a control signal of the first control driver 12a is set to a voltage “0” having a low level. By doing so, the first switching element 3a is turned on, and the first driver 13a is coupled to the transistors 8 included in the first pixel group 6a. At this time, the first latch circuit 4a is turned off.

[0115]At time T1, the second control driver 12b and a third control driver 12c set control signals to a voltage “1” having a high level. By doing so, the second switching element 3b and a third switching element 3c are turned off, and the driver 13 is decoupled from the second pixel group 6b and the third pixel group 6c.

[0116]At time T2, in a state in which the first switching element 3a is turned on, the select signal sel13a “0” which is an inverted signal of the select signal sel13a “1” that operates the select transistor 8a is output from the first driver 13a. The select signal sel13a “0” is inverted to the select signal sel13a “1” by the CMOS inverter 5a included in the first latch circuit 4a, and is input to the select transistor 8a included in the first pixel group 6a. By doing so, the select transistor 8a to which the select signal sel13a “1” is input operates.

[0117]At time T3, in a state in which the first switching element 3a is turned on, the reset signal res13a “0” which is an inverted signal of the reset signal res13a “1” that operates the reset transistor 8b is output from the driver 13. The reset signal res13a “0” is inverted to the reset signal res13a “1” by the CMOS inverter 5a included in the first latch circuit 4a, and is input to the reset transistor 8b included in the first pixel group 6a. By doing so, the reset transistor 8b to which the reset signal res13a “1” is input operates. As the reset transistor 8b operates, the potential of the FD 9 becomes a potential VDD of the power supply terminal 17. After that, the reset voltage is input to the signal processing unit 15 through the vertical signal line 24.

[0118]At time T4, the driver 13 is set to a voltage “0” having a low level, and the reset transistor 8b stops.

[0119]Subsequently, at time T5, in a state in which the first switching element 3a is turned on, the transfer signal tx13a “0” which is an inverted signal of the transfer signal tx13a “1” that operates the transfer transistor 8c is output from the first driver 13a. The transfer signal tx13a “0” is inverted to the transfer signal tx13a “1” by the CMOS inverter 5a included in the first latch circuit 4a, and is input to the transfer transistor 8c included in the first pixel group 6a. By doing so, the transfer transistor 8c to which the transfer signal tx13a “1” is input operates.

[0120]As the transfer transistor 8c operates, the electric charges accumulated in the photo diode 7 are transferred to the FD 9. Accordingly, the FD 9 decreases by a potential corresponding to the electric charges accumulated in the photo diode 7 from the reset potential VDD. The potential is applied to a gate of the amplification transistor 8d as a pixel voltage. The pixel voltage is output to the vertical signal lines 24 through the select transistor 8a, and thereafter, the pixel voltage is input to the signal processing unit 15.

[0121]At time T6 when reading of the electric charges of the photo diode 7 is completed, the third driver 13c outputs the transfer signal “0”. By doing so, the transfer transistor 8c stops. Accordingly, the transfer transistor 8c returns to a reset state.

[0122]Subsequently, at time T7, the control signals of the first control driver 12a and the third control driver 12c are set to a voltage “1” having a high level. Accordingly, at this time, the first switching element 3a and the third switching element 3c are turned off, and the drivers 13 is decoupled from the transistors 8 included in the first pixel group 6a, and the transistors 8 included in the third pixel group 6c.

[0123]In addition, the first latch circuit 4a retains the transfer signal which stops the transfer transistor 8c. Accordingly, the transfer transistor 8c stops, and the reset state is maintained.

[0124]At time T7, the second control driver 12b sets the control signal to a voltage “0” having a low level. Accordingly, the second switching element 3b is turned on, and the first driver 13a is coupled to the transistors 8 included in the second pixel group 6b.

[0125]After that, the transistors 8 perform the same operations as those described above, and thus description thereof will be omitted.

[0126]The solid-state imaging device according to the second embodiment includes the switching element 3 and the latch circuit 4 which are provided on the first semiconductor substrate 1. By doing so, any one or all of the first switching element 3a, the second switching element 3b, and the third switching element 3c which are included in the switching element 3 are turned on, and thereby any one or a of the first pixel group 6a, the second pixel group 6b, and the third pixel group 6c which correspond to those are coupled to the first driver 13a. Accordingly, it is possible for the first driver 13a to operate each pixel group. Since one driver can operate three pixel groups, it is possible to reduce the number of drive signal lines which couple the drivers 13 to the pixel groups. For this reason, it is possible to reduce the number of the coupling portions 25 which are configured by overlapping the first semiconductor substrate 1 with the second semiconductor substrate 10.

[0127]In the solid-state imaging device according to the second embodiment, for example, the number of the coupling portions 25 required to couple the driver 13 and the control unit 12 which are provided on the second semiconductor substrate 10 to the elements which are provided on the first semiconductor substrate 1 can be represented by Expression 2.

[0128]When the number of pixel groups is n, the number T of the coupling portions is represented by Expression 2.

(Expression 2) T=n/(3+3)

[0129]For example, as described in the example of the second

embodiment, in a case of three pixel groups, the number of the coupling portions 25 at the time when the driver 13 and the control unit 12 are coupled to the elements provided on the first semiconductor substrate 1 is four pieces.

[0130]In the second embodiment, only the first driver 13a, the first pixel group 6a, the second pixel group 6b, and the third pixel group 6c are described, but one driver 13 can operate three pixel groups, also in the second driver 13b as well as the first driver 13a, and thus it is possible to reduce the number of the coupling portions 25.

Third Embodiment

[0131]A solid-state imaging device according to a third embodiment will be described with reference to FIG. 9. FIG. 9 is a schematic top diagram illustrating a part of a configuration of a solid-state imaging device according to a third embodiment. The solid-state imaging device according to the third embodiment is different from the solid-state imaging device according to the first embodiment in that one driver can operate an nth pixel group 6 which is disposed in parallel with the first pixel group 6a at a position separated from the first pixel group 6a, for example, in an nth row. FIG. 9 illustrates an example in which the first pixel group 6a in a first row and a fourth pixel group 6d in a fourth row are operated by the first driver 13a.

[0132]When the switching element 3 is turned on, the first pixel group 6a, the second pixel group 6b, the third pixel group 6c, and a fourth pixel group 6d are sequentially operated by a drive signal from the drivers 13. At this time, if the first control driver 12a outputs the control signal which turns on the first switching element 3a, it is not necessary to output the control signal according to switching of the pixel group which operates.

[0133]As described above, according to the solid-state imaging device according to the third embodiment, it is possible to reduce the number of the coupling portions 25, and furthermore, it is possible to decrease an activation rate since it is not necessary to frequently operate the control signal from the control unit 12.

Fourth Embodiment

[0134]A fourth embodiment will be described as a modification example of the first embodiment.

[0135]As illustrated in FIG. 1, a solid-state imaging device according to a fourth embodiment has a stacked structure which is formed by overlapping the first semiconductor substrate 1 with the second semiconductor substrate 10. In the solid-state imaging device having the stacked structure of the related art, one driver provided on the second semiconductor substrate 10 is coupled in one-to-one correspondence with a pixel group provided on the first semiconductor substrate 1. However, when the first semiconductor substrate 1 overlaps the second semiconductor substrate 10, misalignment may occur between the first electrode 25a provided on the first semiconductor substrate 1 and the second electrode 25b provided on the second semiconductor substrate 10. Due to the misalignment, the drive signal may not be sufficiently transferred to the pixel group from the driver, and thus the yield of the solid-state imaging device is reduced. Hence, one driver is coupled to two pixel groups through two electrodes. By using the structure, misalignment at the time of overlapping can be prevented, and when one of the electrodes which are coupled to one driver fails, the other electrode can be used. Accordingly, it is possible to prevent a yield from decreasing.

[0136]The solid-state imaging device according to the fourth embodiment will be described with reference to FIG. 1 and FIG. 10. FIG. 10 is a schematic top diagram illustrating a part of a configuration of the solid-state imaging device according to the fourth embodiment.

[0137]A structure of the fourth embodiment will be described with reference to FIG. 10. Meanwhile, the same symbols or reference numerals will be attached to the same portions as in the first embodiment, and detailed description thereof will be omitted.

[0138]As illustrated in FIG. 10, the first semiconductor substrate 1 includes the pixel area 2, the switching elements 3, the latch circuits 4, the first electrodes 25a, and the second electrodes 25b. The second semiconductor substrate 10 includes the control unit 12, the pixel drive unit 14, the signal processing unit 15, third electrodes 25c, and fourth electrodes 25d. Meanwhile, in the fourth embodiment, an example in which the control unit 12 is provided on the second semiconductor substrate 10 is described, but the control unit 12 may be provided on the first semiconductor substrate 1.

[0139]The pixel area 2 is configured by a plurality of pixels 6 which are disposed in a matrix.

[0140]In the first embodiment, a collection of the pixels 6 which are disposed in a first row of the pixel area 2 is referred to as a first pixel group 6a. A collection of the pixels 6 which are disposed in a second row of the pixel area 2 is referred to as a second pixel group. The second pixel group 6b is disposed in parallel with the first pixel group 6a. In the first embodiment, for the sake of clear description, only the first pixel group 6a and the second pixel group 6b are described, but, in the same manner, a collection of the pixels 6 which are disposed in an nth row is referred to as an nth pixel group.

[0141]The switching element 3 is divided into the first switching element 3a and the second switching element 3b. One terminal of the first switching element 3a is coupled to the first electrode 25a through a first drive signal line 30a which will be described later, and the other terminal of the first switching element 3a is coupled to the first latch circuit 4a. One terminal of the second switching element 3b is coupled to the second electrode 25b through a second drive signal line 30b which will be described later, and the other terminal of the second switching element 3b is coupled to the second latch circuit 4b.

[0142]The latch circuit is divided into the first latch circuit 4a and the second latch circuit 4b. One terminal of the first latch circuit 4a is coupled to the first switching element 3a, the other terminal of the first latch circuit 4a is coupled to the first pixel group 6a. One terminal of the second latch circuit 4b is coupled to the second switching element 3b, and the other terminal of the second latch circuit 4b is coupled to the second pixel group 6b.

[0143]The pixel drive unit 14 provided on the second semiconductor substrate 10 includes drivers. The drivers are disposed such that one driver corresponds to pixel groups in two rows. In the fourth embodiment, an example in which the driver 13 that operates the first pixel group 6a and the second pixel group 6b is referred to as the first driver 13a is described, in the same manner as in the first embodiment. The first driver 13a is coupled to a drive signal line.

[0144]The drive signal line is divided into a first drive signal line 30a and a second drive signal line 30b. The first drive signal line 30a is coupled to a third electrode 25c. The second drive signal line 30b is coupled to a fourth electrode 25d. In a solid-state imaging device having a stacked structure in which the first semiconductor substrate 1 overlaps the second semiconductor substrate 10, the first electrode 25a is coupled to the third electrode 25c, and the second electrode 25b is coupled to the fourth electrode 25d. By doing so, the first drive signal line 30a is coupled to the first pixel group 6a through the first electrode 25a and the third electrode 25c, and the second drive signal line 30b is coupled to the second pixel group 6b through the second electrode 25b and the fourth electrode 25d. By doing so, the first driver 13a can supply a drive signal to the first pixel group 6a through the first drive signal line 30a, and can supply another drive signal to the second pixel group 6b through the second drive signal line 30b.

[0145]A coupling signal line 31 which couples the first drive signal line 30a to the second drive signal line 30b is provided on the first semiconductor substrate 1. A switch which is not illustrated may be provided in the coupling signal line 31. When one of the coupling portion 25 which is configured with the first electrode 25a and the third electrode 25c, and the coupling portion 25 which is configured with the second electrode 25b and the fourth electrode 25d fails, or when misalignment occurs, a drive signal from the first driver 13a can be supplied to either the first pixel group 6a or the second pixel group 6b through the coupling signal line 31 by using the other of the coupling portion.

[0146]In the fourth embodiment, an example in which the first driver 13a operates the first pixel group 6a and the second pixel group 6b is described, but it is also possible for the first driver 13a to operate the first pixel group 6a, the second pixel group 6b, and the third pixel group 6c.

[0147]As described above, by using the above structure, even if one of two coupling portions 25 which couple the first driver 13a to two pixel groups fails, the drive signal from the first driver 13a can be supplied to a pixel group through the other of the coupling portions 25. Accordingly, when the number of pixel groups which are operated by the first driver 13a is increased, only the coupling portion 25 which couples a control driver to the switching element 3 or the like may be increased, while the number of the coupling portions 25 which couple the first driver 13a to each pixel group is maintained.

[0148]In addition, since the first driver 13a can operate each pixel group through a plurality of the coupling portions 25, redundancy of the coupling portion 25 is improved.

[0149]As described above, even if a production yield of the coupling portion 25 decreases, it is possible to prevent a production yield of the solid-state imaging device from decreasing.

[0150]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A solid-state imaging device comprising:

a first pixel group which is provided on a first semiconductor substrate and has pixels including photoelectric conversion elements;

a second pixel group which is provided on the first semiconductor substrate and has pixels including photoelectric conversion elements;

a first electrode which is provided on the first semiconductor substrate;

a first switching element which is provided on the first semiconductor substrate and is coupled to the first electrode;

a first latch circuit which is provided on the first semiconductor substrate and is coupled to the first switching element and the first pixel group;

a second switching element which is provided on the first semiconductor substrate and is coupled to the first electrode;

a second latch circuit which is provided on the first semiconductor substrate and is coupled to the second switching element and the second pixel group;

a second electrode that is provided on a second semiconductor substrate on which the first semiconductor substrate is stacked, and is coupled to the first electrode;

a driver which is provided on the second semiconductor substrate and is coupled to the second electrode; and

a control unit which operates the first switching element, the second switching element, the first latch circuit, and the second latch circuit.

2. The device according to Claim 1, further comprising:

a third pixel group which is provided on the first semiconductor substrate and has pixels including photoelectric conversion elements;

a third switching element which is provided on the first semiconductor substrate and is coupled to the first electrode; and

a third latch circuit which is provided on the first semiconductor substrate and is coupled to the third switching element and the third pixel group,

wherein the control unit operates the third switching element and the third latch circuit.

3. The device according to Claim 1, wherein the control unit includes a first control driver which operates the first switching element and the first latch circuit, and a second control driver which operates the second switching element and the second latch circuit.

4. The device according to Claim 2, wherein the control unit includes a third control driver which operates the third switching element and the third latch circuit.

5. A solid-state imaging device comprising:

a first pixel group which is provided on a first semiconductor substrate and has pixels including photoelectric conversion elements;

a second pixel group which is provided on the first semiconductor substrate and has pixels including photoelectric conversion elements;

a first electrode which is provided on the first semiconductor substrate;

a second electrode which is provided on the first semiconductor substrate;

a first switching element which is provided on the first semiconductor substrate and is coupled to the first electrode through a first drive signal line;

a first latch circuit which is provided on the first semiconductor substrate and is coupled to the first switching element and the first pixel group;

a second switching element which is provided on the first semiconductor substrate and is coupled to the second electrode through a second drive signal line;

a second latch circuit which is provided on the first semiconductor substrate and is coupled to the second switching element and the second pixel group;

a third electrode that is provided on a second semiconductor substrate on which the first semiconductor substrate is stacked, and is coupled to the first electrode;

a fourth electrode which is provided on the second semiconductor substrate and is coupled to the second electrode;

a driver which is provided on the second semiconductor substrate and is coupled to the third electrode and the fourth electrode;

a coupling signal line which is provided on the first semiconductor substrate and couples the first drive signal line to the second drive signal line; and

a control unit which operates the first switching element, the second switching element, the first latch circuit, and the second latch circuit.

6. The device according to any one of Claims 1 to 5, wherein each of the first to third switching elements is a transmission gate in which a PMOS transistor and an NMOS transistor are coupled in parallel with each other.

7. The device according to any one of Claims 1 to 6, wherein the first to third pixel groups are disposed in parallel with each other in a row direction on the first semiconductor substrate.

ABSTRACT

A solid-state imaging device according to an embodiment includes a first pixel group which is provided on a first semiconductor substrate and has pixels including photoelectric conversion elements; a second pixel group which has pixels including photoelectric conversion elements; a first electrode; a first switching element which is coupled to the first electrode; a first latch circuit which is coupled to the first switching element and the first pixel group; a second switching element which is coupled to the first electrode; a second latch circuit which is coupled to the second switching element and the second pixel group; a second electrode that is provided on a second semiconductor substrate on which the first semiconductor substrate is stacked, and is coupled to the first electrode; a driver which is coupled to the second electrode; and a control unit which operates the first switching element, the second switching element, the first latch circuit, and the second latch circuit.